REMARKS

The outstanding Action has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claims 1-19 are pending in this application. By this Amendment, claims 1, 4, and 19 have been amended for clarification. No new matter has been introduced.

Allowable Subject Matter

It is noted with appreciation that claims 2, 3, and 6-17 have not been rejected based on the cited references of record.

Drawing Objection

The drawings are objected to under 37 C.F.R. § 1.83(a) for not showing every feature of the invention specified in the claims.

In response to the Examiner's comments as set forth on page 2 of the outstanding Action, it is respectfully submitted that this objection should be withdrawn since the flip-flop as recited in claim 12 is shown in Fig. 3 (see numeral 41) and discussed, e.g., on page 12 of the specification. Additionally, the date input terminal is shown in Fig. 3 (see RS) and discussed, e.g., on pages 12 and 13 of the specification, and the delay circuit is also shown in Fig. 3 (see numeral 45) and discussed, e.g., on page 22 of the specification.

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Section 112, First Paragraph Rejection

Claims 1-19 are rejected under U.S.C. §112, first paragraph, as containing subject matter which is not described in the specification.

The phrase "current output terminal" and its related limitations have been deleted from claims 1, 4 and 19 to overcome this rejection.

Section 112, Second Paragraph Rejection

Claims 1-19 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

Certain concerns of the Examiner as set forth on page 3 of the outstanding Action have been appropriately addressed by the amendments to claims 1, 4 and 19. The supported for the claim amendments can be found, e.g., on page 10, lines 12-17, and page 14, line 31 to page 15, line 14 of the present application.

Additionally, it is respectfully submitted that the delay circuit is shown in Fig. 3 (see numeral 45) and discussed, e.g., on page 22 of the specification.

Section 102 Rejections

Claims 1, 4, 18 and 19 have been rejected under 35 U.S.C. §102(b) as being anticipated by *Hayashi* (U.S. Patent No. 6,097,227).

The present invention as now set forth in claims 1, 4, 18 and 19 includes a particular feature with respect to a state detecting circuit changing a mode switching signal and switching the mode of a charge pump between a high-speed mode and a

normal mode when the charge pump is in a high impedance state (i.e. non-operating state). Accordingly, the lock-up time due to an unlocked state (lock-off state) is shortened and a high-speed lock-up is achieved.

Hayashi specifically discloses a current generator 30 which sends a control current ICNT to a charge pump 20 based on a signal received from a lock detector 50 (see Fig. 4). ***Hayashi*** simply does not disclose, teach or suggest the claimed feature of a state detecting circuit or a mode control circuit that switches the mode of a charge pump when the charge pump is in a high impedance state.

Claims 1, 4, 18 and 19 are also rejected under 35 U.S.C. § 102(b) as being anticipated by *Fukuda* (U.S. Patent No. 5,831,483, hereinafter "*Fukuda*").

Fukuda specifically discloses a PLL state detector 7 that generates a gain control signal Vg to a charge pump 5 based on signals received from a frequency phase comparator 4 (see Fig. 1). ***Fukuda*** also fails to compensate for the above-discussed deficiency of ***Hayashi*** regarding a state detecting circuit or a mode control circuit that switches the mode of a charge pump when the charge pump is in a high impedance state.

Claims 1, 4, 5, 18 and 19 are also rejected under 35 U.S.C. § 102(e) as being anticipated by *Nam et al.* (U.S. Patent No. 6,226,339, hereinafter "*Nam*").

Nam specifically discloses a current controller 208 that outputs current to a charging pump 201 thorough an output terminal 205 based on an information signal received from a multi-detection circuit 207 (see Fig. 2). As discussed above with

respect to ***Hayashi*** and ***Fukuda***, ***Nam*** also fails to disclose, teach, or suggest the claimed invention as now set forth in claims 1, 4, 18 and 19, which requires a state detecting circuit or a mode control circuit that switches the mode of a charge pump when the charge pump is in a high impedance state.

In light of the discussion above, Applicants respectfully request reconsideration and withdrawal of all objections and rejections, and submit that the present invention as set forth in claims 1-19 is in condition for allowance. If the Examiner believes anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

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Enclosures: Marked-Up Copy of Claim Amendments

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MARKED-UP COPY OF AMENDED CLAIMS

1. (Amended) A method of switching the mode of a PLL circuit, wherein the PLL circuit includes a phase comparator for comparing the phase of a reference frequency-divided signal and the phase of a comparison frequency-divided signal with each other and generating a comparison output signal, a charge pump for generating a current depending on the comparison output signal from the phase comparator, and a voltage-controlled oscillator for generating an output signal having a predetermined frequency in accordance with the current generated by the charge pump, and wherein the PLL circuit has a first mode for locking an output signal thereof up to a desired frequency at a high speed and a second mode in normal use, the method comprising the steps of:

detecting [whether a current output terminal of the charge pump is in] a high impedance state of the charge pump; and

switching the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode when the high impedance state is detected.

4. (Amended) A circuit for controlling the mode of a PLL circuit, wherein the PLL circuit includes a phase comparator for comparing the phase of a reference frequency-divided signal and the phase of a comparison frequency-divided signal with each other and generating a comparison output signal, a charge pump connected to the phase comparator, for generating a current depending on the comparison output signal from the phase comparator, and a voltage-controlled oscillator connected to the charge

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pump, for generating an output signal having a predetermined frequency in accordance with the current generated by the charge pump, and wherein the PLL circuit has a first mode for locking an output signal thereof up to a desired frequency at a high speed and a second mode in normal use, the circuit comprising:

a state detecting circuit for detecting [whether a current output terminal of the charge pump is in] a high impedance state of the charge pump, and generating a mode switching signal to switch the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode when the high impedance state is detected.

19. (Amended) A semiconductor device comprising:

a PLL circuit; and

a mode control circuit connected to the PLL circuit, for controlling switching of the mode of the PLL circuit; wherein the PLL circuit includes:

a phase comparator for comparing the phase of a reference frequency-divided signal and the phase of a comparison frequency-divided signal with each other and generating a comparison output signal,

a charge pump connected to the phase comparator, for generating a current depending on the result of the comparison by the phase comparator, and

a voltage-controlled oscillator connected to the charge pump, for generating an output signal having a predetermined frequency in accordance with the current generated by the charge pump, wherein the PLL circuit has a

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first mode for locking an output signal thereof up to a desired frequency at a high speed and a second mode in normal use; and

wherein the mode control circuit detects [whether a current output terminal of the charge pump is in] a high impedance state of the charge pump, and generates a mode switching signal to switch the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode when the high impedance state is detected.